

US Patent Application No. 10/822,960
Reply to Office Action of March 9, 2006

Attorney Docket No. 2003-1398 / 24061.187
Customer No. 42717

REMARKS

Claims 1, 2, 4-9 and 23-25 are pending in the application, of which claims 7-9 have been allowed. Reconsideration of the pending claims is respectfully requested in light of the following remarks.

Allowable Subject Matter

Claims 7-9 have been allowed.

Rejections Under 35 U.S.C. § 103

Claim 1 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,900,135 to Somekh et al. (hereinafter "Somekh") in view of U.S. Patent No. 6,329,826 to Shinada et al. (hereinafter "Shinada"). Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Somekh in view of Shinada and further in view of U.S. Patent No. 6,410,927 to Pike, hereinafter referred to as "Pike". Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Somekh in view of Shinada and further in view of U.S. Patent No. 6,512,227 to Iwabuchi et al., hereinafter referred to as "Iwabuchi". Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Somekh in view of Shinada and further in view of U.S. Patent No. 6,841,008 to Branco et al., hereinafter referred to as "Branco". Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Somekh in view of Shinada and further in view of U.S. Patent No. 6,355,516 to Kim et al., hereinafter referred to as "Kim". Claim 23 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Somekh in view of Shinada and Pike and further in view of Iwabuchi. Claim 24 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Somekh in view of Shinada and Pike and further in view of Branco. Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Somekh in view of Shinada and Pike and further in view of Kim. Applicants respectfully traverse the subject rejections for the following reasons.

As the PTO recognizes in MPEP § 2142:

... The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness...

It is submitted that, in the present case, the Examiner has not factually supported a prima facie case of obviousness for the following, mutually exclusive, reasons.

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1. Even when combined, the references do not teach the claimed subject matter.

The Somekh and Shinada patents cannot be applied to reject claim 1 under 35 U.S.C. §103(a) because, even when combined, the references do not produce the claimed subject matter.

Claim 1 recites:

*A method of manufacturing a microelectronic device, comprising:
performing a first inspection of a device feature formed on a substrate during an intermediate stage of manufacture;
cleaning the device feature after the first inspection; and
performing a second inspection of the device feature after cleaning the device feature, wherein the first and second inspections are performed by a single inspection tool.*

As conceded by the Examiner, Somekh fails to teach “a device feature formed on a substrate” as recited in claim 1. As a result, Somekh fails to teach “performing a first inspection of a device feature”, “cleaning the device feature”, and “performing a second inspection of the device feature.” The Examiner has taken the position that Shinada remedies the deficiencies of Somekh in this regard. Applicants respectfully traverse the Examiner’s position and submit that, assuming *arguendo* that Shinada is properly combinable with Somekh, the combination teaches, at best, only inspecting a device feature. While Shinada generally recognizes that a wafer is cleaned during production (see column 26, lines 9-44), it is completely devoid of any teaching of cleaning a device feature between inspections, as required by claim 1.

In particular, as evidenced by the section of Shinada cited by the Examiner (column 11, line 26, through column 12, line 10), the focus of Shinada is on “inspecting a substrate having a circuit pattern, for example, such as a semiconductor device” such that defects therein can be detected at an early stage. Applicants submit that the combination of Somekh and Shinada result in a process including, at most, performing an inspection of a device feature, cleaning the backside of the wafer on which the device feature is formed subsequent to the first inspection, and performing a second inspection of the device feature after cleaning the backside of the wafer.

Thus, for this mutually exclusive reason, the Examiner’s burden of factually supporting a *prima facie* case of obviousness has clearly not been met, and the rejection of claim 1 under 35 U.S.C. §103 should be withdrawn.

The Somekh, Pike, and Shinada patents cannot be applied to reject claim 2 under 35 U.S.C. § 103(a) because, even when combined, the references do not produce the claimed subject matter.

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Claim 2, as amended, recites:

*A method of manufacturing a microelectronic device, comprising:
performing a first inspection of a device feature formed on a substrate during an intermediate stage of manufacture;
cleaning the device feature after the first inspection; and
performing a second inspection of the device feature after cleaning the device feature,
wherein the first inspection is performed by a first inspection tool and the second inspection is performed by a second inspection tool different than the first inspection tool.*

For the reasons indicated above with respect to the allowability of claim 1, the combination of Somekh and Shinada, even if proper, fails to teach, suggest, or render obvious "cleaning the first device feature after the first inspection", as recited in claim 2. Pike, which is cited by the Examiner for its teaching of performing first and second inspections using two different inspection tools, fails to remedy the deficiencies of Somekh and Shinada in this regard.

Thus, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness has clearly not been met, and the rejection of claim 2 under 35 U.S.C. §103 should be withdrawn.

2. The combination of references is improper.

§2142 of the MPEP also provides:

...the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made. . . . The examiner must put aside knowledge of the applicant's disclosure, refrain from using hindsight, and consider the subject matter claimed 'as a whole'.

In the case of claim 1, neither Somekh nor Shinada teaches, or even suggests, the desirability of combining a process for cleaning the backside of a wafer, as taught by Somekh, with a process for inspecting a device feature disposed on the topside of the wafer, as taught by Shinada. On the contrary, as pointed out in Somekh, examination and cleaning of the backside of a wafer during manufacturing presents certain unique problems that are specifically addressed by the invention described in that reference. Thus, the invention of Somekh is specifically directed toward those problems and cannot appropriately be combined with a reference directed to a process of inspecting a device feature, which is disposed on the topside of a wafer.

Additionally, in the case of claim 2, none of the cited references (Somekh, Shinada and Pike) teaches, or even suggests, the desirability of combining the use of two different inspection tools, as taught by Pike, with the teachings of Somekh/Shinada combination. On the contrary, it would appear from the

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teachings of Somekh that a primary benefit of the invention of Somekh is that the cleaning and inspection may be performed using a single tool. Therefore, it would be antithetical to the teachings of Somekh to perform a second inspection using a second, and different, tool, as described in Pike.

Thus, it is clear that neither patent provides any incentive or motivation supporting the desirability of the combination. Therefore, there is simply no basis in the art for combining the references to support a 35 U.S.C. §103 rejection.

In this context, the MPEP further provides at § 2143.01:

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.

In the above context, the courts have repeatedly held that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination.

In the present case it is clear that the Examiner's combination arises solely from hindsight based on the invention without any showing, suggestion, incentive or motivation in either reference for the combination as applied to claims 1 and 2. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness has clearly not been met, and the rejection under 35 U.S.C. §103 should be withdrawn.

Claims 4-6 depend from and further limit independent claim 1, in a patentable sense, and are therefore deemed to be in condition for allowance for the reasons set forth above with respect to the allowability of claim 1.

Claims 23-25 depend from and further limit independent claim 2, in a patentable sense, and are therefore also deemed to be in condition for allowance for the reasons set forth above with respect to the allowability of claim 2.

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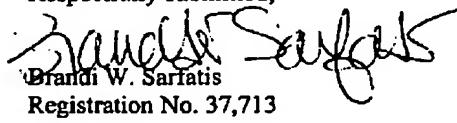
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Conclusion

Claims 7-9 have been allowed. For the reasons set forth in detail above, claims 1 and 2 are deemed to be in condition for allowance. Claims 4-6 and 23-25 depend from and further limit independent claims 1 and 2 and are therefore also deemed to be in condition for allowance. Accordingly, Applicants respectfully request that the Examiner withdraw the pending rejections and issue a formal notice of allowance.

An early formal notice of allowance of claims 1, 2, 4-6, and 23-25 is respectfully requested.

Respectfully submitted,


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Dated: 4/6/06

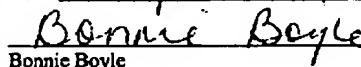
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